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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,019	01/16/2004	Lih-Chung Kuo	IBMS.070PA(0511)	8505

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EXAMINER	
BORKOWSKI, ROBERT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,019	KUO ET AL.	
	Examiner	Art Unit	
	Robert Borkowski	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/16/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-9, 11-25, 27-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Creta et al. (U.S. Patent Application Publication No. 2004/0193757 A1) in view of Collier et al. (U.S. Patent No. 6,975,593 B2).

Regarding claims 1, 11, 27-29, Creta et al. teaches a method for managing dataflow through a processing system comprising:

a processor (Fig. 1 element 102);

gathering writes in a buffer (paragraph 0004, Fig. 1) before transmitting a burst of writes over an external bus (paragraph 0023, Fig. 1);

monitoring the buffer (paragraphs 0022, 0032, Fig. 2) to determine a number of writes in the buffer and whether the number of writes in the buffer exceed a predetermined threshold (paragraph 0032, Fig. 2). However, Creta et al. is silent

wherein providing control over writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold.

Collier et al. discloses wherein providing control (see Collier column 1 lines 42-63) over writes provided to the buffer in response to the monitored number of writes in the buffer (see Collier column 2 lines 45-67) and the predetermined threshold (see Collier column 1 line 56 thru column 2 line 4).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Creta et al. use control over writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it (see Collier column 1 lines 13-19).

It is for this reason that one of ordinary skill in the art be motivated to implement Creta et al. method with control over writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it.

Regarding claims 2, 24, Creta et al. is silent wherein the providing control further comprises slowing writes to the buffer when the writes in the buffer exceed the predetermined threshold. However, Collier et al. discloses wherein the providing control

further comprises slowing writes (see Collier column 2 lines 5-13) to the buffer when the writes in the buffer exceed the predetermined threshold (see Collier column 1 lines 56-63).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Creta et al. use control to slow writes to the buffer when the writes in the buffer exceed the predetermined threshold in response to the monitored number of writes in the buffer and the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it (see Collier column 1 lines 13-19).

It is for this reason that one of ordinary skill in the art be motivated to implement Creta et al. method with control to slow writes to the buffer when the writes in the buffer exceed the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it.

Regarding claim 3, Creta et al. teaches wherein the gathering writes in a buffer (paragraph 0004, Fig. 1) before transmitting a burst or writes over an external bus further comprising transmitting a burst of writes over a bus (paragraph 0023, Fig. 1).

Regarding claims 4, 15, 22-23, Creta et al. is silent on initiating error recovery in response to the writes in the buffer exceeding the predetermined threshold. However, Collier et al. discloses initiating error recovery in response to the writes in the buffer exceeding the predetermined threshold (see Collier column 4 lines 39-59).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Creta et al. use initiating error recovery in response to the writes in the buffer exceeding the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it (see Collier column 1 lines 13-19).

It is for this reason that one of ordinary skill in the art be motivated to implement Creta et al. method with initiating error recovery in response to the writes in the buffer exceeding the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it.

Regarding claims 5, 16-18, Creta et al. is silent wherein providing an arbitration signal for controlling access to the external bus in response to the comparison of the writes in the buffer to the predetermined threshold. However, Collier et al. discloses an arbitration signal for controlling access to the external bus in response to the comparison of the writes in the buffer to the predetermined threshold (see Collier column 1 line 56 thru column 2 line 4).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Creta et al. use an arbitration signal for controlling access to the external bus in response to the comparison of the writes in the buffer to the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the

sending device is capable of sending data faster than the receiving device can use it (see Collier column 1 lines 13-19).

It is for this reason that one of ordinary skill in the art be motivated to implement Creta et al. method with an arbitration signal for controlling access to the external bus in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it.

Regarding claim 6-7, 19-21, Creta et al. is silent wherein the providing control over writes provided to the buffer further comprises providing a vector to a register and scanning the register for the vector to determine when to slow writes to the buffer. However, Collier et al. discloses wherein the providing control over writes provided to the buffer further comprises providing a vector to a register (see Collier column 3 line 62 thru column 4 line 17, Fig. 2) and scanning the register (see Collier column 3 line 62 thru column 4 line 17, Fig. 2) for the vector to determine when to slow writes to the buffer (see Collier column 2 lines 5-13).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Creta et al. use control over writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it (see Collier column 1 lines 13-19).

It is for this reason that one of ordinary skill in the art be motivated to implement Creta et al. method with control over writes to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it.

Regarding claims 8, 25, Creta et al. teaches clearing the buffer (paragraphs 0032-0034, 0042, Fig. 6), Creta et al. is silent regarding clearing the buffer when the writes in the buffer exceed the predetermined threshold. However, Collier et al. discloses clearing the buffer when the writes in the buffer exceed the predetermined threshold (see Collier column 1 line 56 thru column 2 line 4).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Creta et al. use of clearing the buffer when the writes in the buffer exceed the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it (see Collier column 1 lines 13-19).

It is for this reason that one of ordinary skill in the art be motivated to implement Creta et al. method with an arbitration signal for clearing the buffer when the writes in the buffer exceed the predetermined threshold in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it.

Regarding claim 9, Creta et al. teaches clearing the buffer (paragraphs 0032-0034, 0042, Fig. 6), Creta et al. is silent regarding wherein a timeout signal is provided for indicating when a transaction is not cleared from the buffer within a predetermined amount of time. However, Collier et al. discloses a timeout signal (see Collier column 2 lines 45-67) for indicating when a transaction is not cleared from the buffer within a predetermined amount of time (see Collier column 2 lines 45-67).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Creta et al. use of a timeout signal indicating when a transaction is not cleared from the buffer within a predetermined amount of time in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it (see Collier column 1 lines 13-19).

It is for this reason that one of ordinary skill in the art be motivated to implement Creta et al. method with a timeout signal indicating when a transaction is not cleared from the buffer within a predetermined amount of time in order to ensure that the receiving device can handle all of the incoming data, especially when the sending device is capable of sending data faster than the receiving device can use it.

Regarding claims 12-13, Creta et al. discloses wherein the external bus comprises a PCI-X bus (paragraph 0043, Fig. 1).

Regarding claim 14, Creta et al. discloses a processor interface coupled to the buffer, the processor interface linking the buffer to a processor bus (Fig. 1).

3. **Claims 10, 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Creta et al. (U.S. Patent Application Publication No. 2004/0193757 A1) in view of Azevedo et al. (U.S. Patent No. 6,496,890 B1).

Regarding claims 10, 26, Creta et al. is silent on determining whether an external interface is hung and clearing the buffer and external bus transaction when an external interface is hung. However, Azevedo et al. discloses determining whether an external interface is hung and clearing the buffer and external bus transaction when an external interface is hung (see Azevedo Abstract, column 2 line 60 thru column 3 line 45, Fig. 3).

One of the ordinary skill in the art at the time of applicant's invention would have clearly recognize that it is quiet advantageous for the method of Creta et al. determine whether an external interface is hung and clearing the buffer and external bus transaction when an external interface is hung in order to ensure that the configuration should minimize the amount of time that data from a particular source must wait to be read or write, and that the latency should be minimized (see Azevedo column 4 lines 29-44).

It is for this reason that one of ordinary skill in the art be motivated to implement Creta et al. method with determining whether an external interface is hung and clearing the buffer and external bus transaction when an external interface is hung in order to ensure that the configuration should minimize the amount of time that data from a particular source must wait to be read or write, and that the latency should be minimized.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents have been made of record of to further show the dataflow control methods.

1) Heath et al. U.S. Patent No. 4,258,418

2) Suzuki et al. U.S. Patent No. 4,285,038

3) Shrock et al. U.S. Patent No. 5,455,913

4) Paul et al. U.S. Patent No. 5,778,175

5) Joung et al. U.S. Patent No. 6,628,613

6) Park et al. U.S. Patent No. 6,646,985

7) Bullis et al. U.S. Patent No. 6,876,664

8) Payson et al. U.S. Patent Application Publication No. 2005/0259748 A1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert Borkowski whose telephone number is 571-272-8626. The examiner can normally be reached on Monday - Friday 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM NGOC (KIM) HUYNH can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert Borkowski
Art Unit 2181
February 7, 2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/8/06